WHAT IS CLAIMED IS:

1. A time limit function utilization apparatus, comprising:

a first functional block;

a second functional block;

a signal line which connects the first functional block and the second functional block and allows using a desired function that is generated by accessing the first functional block and the second functional block with each other; and

a semiconductor time switch which is interposed in or connected to the signal line, and substantially disables or substantially enables mutual access between the first functional block and the second functional block upon a lapse of a first predetermined time.

2. The apparatus according to claim 1, wherein the semiconductor time switch substantially disables the mutual access between the first functional block and the second functional block upon the lapse of the first predetermined time, and substantially enables the mutual access between the first functional block and the second functional block upon a lapse of a second predetermined time after an end of the lapse of the first predetermined time.

3. The apparatus according to claim 1, wherein the semiconductor time switch substantially enables the mutual access between the first functional block and

the second functional block upon the lapse of the first

predetermined time, and substantially disables the

mutual access between the first functional block and

the second functional block upon a lapse of a second

5 .predetermined time after an end of the lapse of the

first predetermined time.

4. The apparatus according to claim 1, wherein

the second functional block is a 1st internal circuit

which stores information or a function.

10 5. The apparatus according to claim 4, wherein

the second functional block further comprises (N-1)

internal circuits in addition to the 1st internal

circuit, and

when a definition is made such that, regarding a

15 switch characteristic, a first polarity is one of a

first switch action "on" to "off" and a second switch

action "off" to "on", and a second polarity is the

other of the first switch action and the second switch

action,

20 the semiconductor time switch includes (N-1) first

polarity time switches, (N-1) second polarity ordinary

switches, and (N-1) first polarity ordinary switches,

1st one of the second polarity ordinary switches

is connected between the 1st internal circuit and the

25 first functional block, one terminal of nth one of the

second polarity ordinary switches is connected to the

nth internal circuit, where n is a natural number,

nth one of the first polarity ordinary switches is
connected between the other terminal of the nth one of
second polarity ordinary switches and a terminal of
(n+1)th one of the second polarity ordinary switches,

5   where n is less than N-1,

nth one of the first polarity time switches
simultaneously drives the nth one of the second
polarity ordinary switches and the nth one of the first
polarity ordinary switches, where n is N-1 or less,

10   (N-1)th one of the first polarity ordinary
switches is connected between (N-1)th one of the second
polarity ordinary switches and Nth one of the internal
circuits, and

the first polarity time switches operate

15   sequentially from the 1st one to the (N-1)th one of the
first polarity time switches.

6. The apparatus according to claim 4, wherein
the second functional block further comprises (N-1)
internal circuits in addition to the 1st internal

20   circuit, and

the semiconductor time switch comprises (N)
automatic turn-off time switches and (N-1) automatic
turn-on time switches,

nth one of the automatic turn-off time switch is

25   connected to nth one of the internal circuits, where n
is a natural number,

the nth automatic turn-on time switch is connected

between the nth automatic turn-off time switch and the (n+1)th automatic turn-off time switch, where n is N-1 or less, and

the automatic turn-off time switches operate sequentially from the 1st one to Nth one and the automatic turn-on time switches operate sequentially from the 1st one to the (N-1)th one in synchronism with the same ordinal number's one of the automatic turn-off time switches.

7. The apparatus according to claim 1, further comprising:

a first input/output terminal provided on a midpoint of the signal line, the first functional block and one terminal of the semiconductor time switch being connected to the first input/output terminal; and

a third functional block connected to the other terminal of the semiconductor time switch.

8. The apparatus according to claim 7, wherein,

when a definition is made such that, regarding a switch characteristic, a first polarity is one of a first switch action "on" to "off" and a second switch action "off" to "on", and a second polarity is the other of the first switch action and the second switch action,

the semiconductor time switch comprises:

a second polarity ordinary switch connected between the input/output terminal and the second

functional block,

a first polarity ordinary switch connected between the input/output terminal and the third functional block, and

5 a first polarity time switch simultaneously driving the second polarity ordinary switch and the first polarity ordinary switch.

9. The apparatus according to claim 7, wherein when a definition is made such that, regarding a

10 switch characteristic, a first polarity is one of a first switch action "on" to "off" and a second switch action "off" to "on", and a second polarity is the other of the first switch action and the second switch action,

15 the semiconductor time switch comprises:

a second polarity time switch connected between the input/output terminal and the second functional block, and

a first polarity time switch connected between the

20 input/output terminal and the third functional block.

10. The apparatus according to claim 1, wherein the semiconductor time switch comprises a source region and a drain region formed apart from each other on a semiconductor layer, and a gate electrode

25 insulatively formed on a channel region between the source region and the drain region,

the source region and the drain region are used as

two connection terminals of the semiconductor time
switch, and

one of the source region and the drain region is
connected to the first functional block and the other
of the source region and the drain region is connected
to the second functional block.

11.   The apparatus according to claim 10, wherein
in the semiconductor time switch, the channel region
between the source region and the drain region is
rendered conductive or nonconductive by supplying
charges to the gate electrode in advance, the charges
are removed from the gate electrode over time, and the
channel region between the source region and the drain
region is rendered nonconductive or conductive upon the
lapse of the first predetermined time.

12.   The apparatus according to claim 11, wherein
the charges are injected into or leak from the gate
electrode via one selected from the group consisting of
a p-n junction, a pnp junction, an n^+nn^+ junction, a
p^+pp^+ junction, an npn junction, and a Schottky
junction.

13.   The apparatus according to claim 11, wherein
the gate electrode is covered with an insulating
member, and the charges are injected into or leak from
the gate electrode via the insulating member.

14.   A semiconductor integrated circuit comprising:
an aging circuit configured by parallel-connecting

a plurality of aging devices in which an age-based

change occurs while a power supply is disconnected, and

an output signal sensed in read changes over time; and

a sense circuit comparing the output signal from

5   the aging circuit with a reference signal.

15.   The circuit according to claim 14, wherein

when a time until an output signal from each of the

aging devices reaches a predetermined level is defined

as a life time of each of the aging devices and a time

10   until the output signal from the aging circuit reaches

a level of the reference signal is defined as a life

time of the aging circuit, the level of the reference

signal is so set as to make the life time of the aging

circuit longer than an average life time of the aging

15   devices.

16.   The circuit according to claim 14, wherein a

level of the reference signal is set to a value smaller

by a predetermined offset amount than a value at which

the output signal from the aging circuit is maximized

20   upon a lapse of a time, or a value larger by a

predetermined offset amount than a value at which the

output signal from the aging circuit is minimized upon

a lapse of a time.

17.   The circuit according to claim 14, which

25   further comprises a memory that stores the reference

signal, and in which a level of the reference signal

stored in the memory is adjusted to control a life time

of the aging circuit.

18. The circuit according to claim 14, wherein the aging device has a charge accumulation layer accompanied by leakage while the power supply is disconnected.

19. The circuit according to claim 14, wherein the aging device is configured by series-connecting a plurality of field effect devices each having a charge accumulation layer accompanied by leakage while the power supply is disconnected.

20. The circuit according to claim 14, wherein

the aging circuit comprises a first sub-aging circuit configured by parallel-connecting a plurality of first aging devices in which the output signal decreases over time, and a second sub-aging circuit configured by parallel-connecting a plurality of second aging devices in which the output signal increases over time,

the first sub-aging circuit and the second sub-aging circuit are series-connected, and

when a time until the output signal from the first sub-aging circuit reaches a first predetermined level is defined as a life time of the first sub-aging circuit and a time until the second sub-aging circuit reaches a second predetermined level is defined as a life time of the second sub-aging circuit, the life time of the first sub-aging circuit is longer than the

life time of the second sub-aging circuit.

21. The circuit according to claim 14, wherein the aging circuit comprises a first sub-aging circuit configured by parallel-connecting a plurality of first aging devices in which the output signal decreases over time, and a second sub-aging circuit configured by parallel-connecting a plurality of second aging devices in which the output signal increases over time,

the first sub-aging circuit and the second sub-aging circuit are parallel-connected, and

when a time until the output signal from the first sub-aging circuit reaches a predetermined level is defined as a life time of the first sub-aging circuit and a time until the second sub-aging circuit reaches the predetermined level is defined as a life time of the second sub-aging circuit, the life time of the first sub-aging circuit is shorter than the life time of the second sub-aging circuit.

22. The circuit according to claim 14, further comprising a memory area where correspondence codes of the output signal from the aging circuit and lapsed times are stored in advance, and

the sense circuit compares the output signal from the aging circuit with the correspondence codes stored in the memory area, and senses a lapsed operation time of the aging circuit.

23. The circuit according to claim 14, wherein the aging circuit comprises N sub-aging circuits each having a different life time from others defined by a time until an added output signal within each of the N

5 sub-aging circuits reaches a predetermined-reference signal set for each of the N sub-aging circuits, and

the sense circuit compares the added output signal from each of the N sub-aging circuits with the predetermined reference signal, and senses whether or

10 not each of the N sub-aging circuit closes a life time thereof.

24. The circuit according to claim 23, wherein

each of the N sub-aging circuits has the different life time from others by a predetermined time which is

15 obtained by dividing, by N, a difference between the shortest life time and the longest life time among the N sub-aging circuits, and

the sense circuit senses a lapsed operation time of the aging circuit by sensing each of the life times

20 of the N sub-aging circuits.

25. A semiconductor integrated circuit comprising:

a plurality of aging devices in which an age-based change occurs while a power supply is disconnected, and output signals sensed in read change over time;

25 a plurality of operational circuits arranged in correspondence with the plurality of aging devices, and having at least three terminals, respectively, first

terminals of which receive the output signals from the plurality of aging devices;

a plurality of first memory areas electrically connected to second terminals of the plurality of operational circuits, respectively, and each storing at least one predetermined signal level;

an adder electrically connected to third terminals of the plurality of operational circuits and adding the output signals from the plurality of operational circuits appearing at the third terminals;

a plurality of circuit breakers which cut off output signals from the plurality of aging devices before the adder receives the output signal on the basis of operational results of the plurality of operational circuits that are obtained by comparing the output signals from the plurality of aging devices with the at least one predetermined signal level;

a second memory area where a predetermined reference signal is stored, and

a sense circuit which compares an output signal from the adder and the reference signal stored in the second memory.

26. The circuit according to claim 25, wherein each of the plurality of circuit breakers includes a trimming transistor with a two-layered gate structure which has a first diffusion layer and a second diffusion layer formed apart from each other on a

semiconductor substrate, a first gate electrode formed

via a first insulating film on the semiconductor

substrate between the first diffusion layer and the

second diffusion layer, and a second gate electrode

5   formed on the first gate electrode via a second gate

insulating film, the first diffusion layer being

electrically connected to a corresponding one of the

output terminals of the plurality of aging devices,

the second diffusion layer of the trimming

10   transistor is electrically connected to a corresponding

one of the first terminals of the plurality of

operational circuits,

the plurality of the operational circuits have

forth terminals, respectively, and the second gate

15   electrode of the trimming transistor is electrically

connected to a corresponding one of the fourth

terminals of the plurality of operational circuits, and

the plurality of operational circuits compare the

output signals of the plurality of aging devices via

20   the trimming transistor with the signal level stored in

the first memory areas, and inject charges into or emit

the charges from the first gate electrode of the

trimming transistor on the basis of a comparison

result.

25   27. The circuit according to claim 26, wherein

each of the plurality of aging devices comprises a

third diffusion layer and a fourth diffusion layer

formed apart from each other on a semiconductor

substrate, a third gate electrode formed via a third

insulating film on the semiconductor substrate between

the third diffusion layer and the fourth diffusion

5   layer, and a fourth gate electrode formed on the third

gate electrode via a fourth gate insulating film,

one of the third diffusion layer and the fourth

diffusion layer of each of the plurality of aging

devices is shared with the first diffusion layer of the

10   trimming transistor, and

a film thickness of the third gate insulating film

of each of the plurality of aging devices is smaller

than a film thickness of the first gate insulating film

of the trimming transistor.

15   28.   The circuit according to claim 25, wherein

each of the plurality of circuit breakers includes

a trimming transistor having a first diffusion layer

and a second diffusion layer formed apart from each

other on a semiconductor substrate, a first gate

20   electrode formed via a first insulating film on the

semiconductor substrate between the first diffusion

layer and the second diffusion layer, the first

diffusion layer being electrically connected to an

output terminal of a corresponding one of the aging

25   devices, and

the plurality of operational circuits compare

the output signals of the aging devices each input via

the trimming transistor with the signal level stored in the first memory areas, and cut, on the basis of a comparison result, electrical connection between a corresponding one of the plurality of operational circuits and the trimming transistor or electrical connection between the corresponding one of the plurality of operational circuits and an adder.

29. The circuit according to claim 25, wherein each of the plurality of circuit breakers includes a cutting trace at which interconnection between a corresponding one of the third terminals of the operational circuits and the adder or between the corresponding pair of the plurality of aging devices and the plurality of operational circuits is cut.

30. The circuit according to claim 25, further comprising a plurality of third memory areas where a result of comparing by the operational circuits the output signals of the aging devices input into the operational circuits and the predetermined signal level(s) stored in the first memory areas is stored, wherein

each of the plurality of circuit breakers includes a trimming transistor which has a first diffusion layer and a second diffusion layer formed apart from each other on a semiconductor substrate, a first gate electrode formed via a first insulating film on the semiconductor substrate between the first diffusion

layer and the second diffusion layer, the first diffusion layer being electrically connected to an output terminal of a corresponding one of the aging devices.

5   31.   The circuit according to claim 25, wherein when a time until each of the output signals of the plurality of aging devices reaches the predetermined signal level stored in the first memory areas is defined as a life time of each of the plurality of

10   aging devices, and a time until the output signal from the adder reaches a level of the reference signal stored in the second memory area is defined as a life time of the aging circuit, the life time of the aging circuit is controlled by adjusting the predetermined

15   signal level stored in the first memory areas.